R E M A R K S

This is a full and timely response to the Office Action mailed August 10, 2007.

Applicants believe that the currently pending claims are not anticipated by or obvious over the cited references for at least the reasons set forth below and respectfully request reconsideration.

Claim Rejections - 35 U.S.C. 112

Claims 1, 3, 5, 6 and 22 have been rejected under 35 U.S.C. 112, second paragraph, as being indefinite.

Claims 1 and 22 are rejected as being unclear due to the term "agent". The term agent is clearly defined in Applicants' specification at page 5, lines 8-16 as follows:

> "The term "agent" is used herein to refer to any component of a system that receives incoming signals or transactions and generates outgoing signals or events as a result, wherein expected values or states of the outgoing signals may be determined based on the incoming transactions, possibly in connection with other information, before the actual outgoing signals are generated by the agent. In one exemplary embodiment, the agent comprises a memory agent in a computer system."

Applicants respectfully believe that the explicit definition of the term in the description is clear, namely, that the agent is a system component that generates outgoing signals based on incoming signals. An exemplary agent is a memory agent in a computer system, such as a processor (page 9, line 25) and other components that generate and handle memory operations or transactions that access various memory or cache deices. (See Background) For example, as described in the

background at page 1, lines 27-29 regarding a computer system having multiple memories, "memory agents work together to determine the source from which the line of memory should be read for the processor". Thus, Applicants believe that the term "agent" has been clearly defined in the specification as a system component that processes memory transactions and would therefore generally be a circuit, although it could be implemented as a computer program.

Claim 3 was rejected because the phrase "corresponding expected output signal" was indicated to be ambiguous. Claim 3 has been amended and is believed to be clear.

Claims 5 and 6 have been rejected because the Examiner believes that the terms "event" and "expectation" in the claims 5 and 6 do not correspond with their descriptions in pages 6-8 of the specification. Applicants respectfully disagree, and see no conflict between these terms as they are used in the claims and in the specification. For example, the term "event" is defined at page 7, lines 17-19 as "any output from the agent under test, which generally should be triggered by a 'stimulus'." As a stimulus is received by an agent under test, such as a request to read a line of memory (page 6, line 28), the checker generates an expectation that a specific event will take place in the future, that is, that the agent under test will generate a read request to a cache. (Page 6, line 30). Applicants respectfully disagree that the use of the terms is inconsistent between the claims and the description, and request that the Examiner specifically point out any perceived inconsistencies. Applicants believe that the claims, as amended, are clear and definite and respectfully requests that the rejections be withdrawn.

Claim Rejections - 35 U.S.C. 101

Claims 1, 4 and 22 have been rejected under 35 U.S.C. 101 as being drawn to non-statutory subject matter for lacking tangible results. Claims 1, 4 and 22 have been amended as requested to recite the tangible result of signaling an error. Support for the amendment is found at page 8, lines 3-6 and in originally filed claim 5. No new matter has been added.

Claim Rejections - 35 U.S.C. 102(b)

Claims 1-20 have been rejected under 35 U.S.C. 102(b) as being anticipated by Goto, U.S. Patent No. 5,617,429. Applicants believe that the claims as amended are allowable over Goto and respectfully request reconsideration. Independent claims 1, 4 and 22 as amended generate expected outputs based at least in part on the input signals detected at the input of an agent being tested. In contrast, Goto predetermines the test inputs and expected outputs, and does not generate the expected outputs based on the detected inputs. Rather, Goto establishes in advance, before the test begins, the input patterns to be tested and their corresponding expected output pattern as described at col. 12, lines 26-33 and col. 12, line 53 - col. 13, line 3:

> "Next, the CPU 103 writes the input pattern to be tested into the input pattern storage 45 through the control bus 56 and the data bus 34. The expected pattern corresponding to the input pattern stored in the input pattern storage 45 is written in the expected pattern storage 52 at the address corresponding to that of the input pattern storage 45. Then, the CPU 103 sets the error processing circuit 7 in an enable state, thereby ensuring self-test mode.
>
> ...

> The decoder 50 decodes the code including the information as to whether agreement or disagreement and the code representing the address of the input pattern storage 45 which stores the input pattern through the signal conductor 48 and selectively outputs the expected pattern of the expected pattern storage 52 having the address. One of a plurality of expected patterns stored in the expected pattern storage 52 is thereby selected, and the expected pattern is outputted through the output signal conductor 53 to the comparator 6. The comparator 6 compares the output signal from the random logic unit 2 with the expected pattern outputted from the expected pattern storage 52, and outputs the comparison result indicating whether agreement or disagreement to the signal conductor 49."

Thus, Goto's expected patterns are not generated based on the input pattern, but are generated in advance with the input patterns. Goto's expected patterns are merely selected, chosen from a pre-populated memory, according to the input pattern. Goto specifically describes this storage of input test patterns and the corresponding expected output patterns at col. 13, lines 17-34, along with a teaching that the inputs and expected outputs should be changed periodically in order to obtain statistical information on the occurrence of error on all possible patterns. The claimed invention does not require that expected output patterns be generated in advance and stored in a memory. The claimed invention enables a circuit or a design to be tested using a software simulation of an architecture at any stage of a design (see page 5, line 33 to page 6, line 2). The software simulation of the architecture in the checker is thus used to generate expected output patterns during operation based on the inputs to the agent being tested, in contrast to Goto's full generation and storage of test inputs and expected outputs in advance.

In view of the above, all of the claims are believed to be in condition for allowance, and Applicants respectfully request that a timely Notice of Allowance be issued.

Respectfully submitted,
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